REMARKS

Claims 1-22 are pending in the application.

Claims 1-4, 10-16, 18, 19, 21 and 22 are rejected as unpatentable over TAGUSA et al. 5,946,065 in view of SEO et al. 6,445,435 and further in view of applicants' disclosed prior art.

Reconsideration and withdrawal of the rejection are respectfully requested because the references do not teach or suggest a plurality of control electrodes each disposed under a gap between adjacent pixel electrodes and over a gate line, as seen in plan view, the control electrode directly overlying the gate line as recited in claim 1 of the present application.

As noted in the Official Action, TAGUSA et al. do not teach a control electrode disposed in a gap between adjacent pixel electrodes and directly overlying the gate line. Applicants' disclosed prior art as shown in Figure 9 does not teach or suggest this feature.

The position set forth in the Official Action is that SEO et al. teach an LCD where each control electrode is disposed above a gate electrode line between adjacent pixel regions. Figures 2A, 2B and reference 125 are indicated as providing support for this teaching. However, this assertion is not supported by what is disclosed by SEO et al.

Specifically, column 3, lines 54-59 of SEO et al. teach that gate lines 101, 101' and data lines 102, 102' define a

unit pixel region. However, applicants are unable to discern an actual pixel electrode as required by claim 1. It is therefore not apparent whether a single electrode sheet is between a plurality of gate lines such that the electrode extends over the gate lines or whether the electrode would be between the boundary defined by the gate lines and the data lines or whether there would be partial overlap between the pixel electrode and either the gate lines or the data lines. Applicants' representative contacted Examiner Wang for clarification of the pixel electrode of SEO et al. Examiner Wang indicated that according to the abstract of SEO et al., the pixel would be between the gate and bus lines.

Based on the interpretation of the pixel electrode being between the gate lines and the data lines, such interpretation would exclude an overlap of the pixel electrode with the data lines or gate lines. Therefore, it is not apparent why one of ordinary skill in the art would combine SEO et al. with TAGUSA et al. since column 25, lines 48-57 of TAGUSA et al. teach that it is advantageous that the pixel electrodes overlap the data lines to improve the contrast. Since one of ordinary skill in the art would want to improve the contrast, it would appear that an overlap of the pixel electrode and the data lines would be required. Since the region between the data lines and the gate lines excludes an overlap of the data lines and the gate

lines, as taught by SEO et al., one of ordinary skill in the art would not combine SEO et al. with TAGUSA et al.

In addition, the capacitor structure of SEO et al. is based on a group of electrodes (common electrode 109, data electrode 108 and gate line 101). As seen in Figure 4 of TAGUSA et al., for example, the storage capacitor counter electrode 27 and the gate electrode 32 are both formed on the substrate 31 such that electrode 27 and gate electrode 32 are in the same plane. Storage capacitor electrode 25a is then formed over storage capacitor counter electrode 27 while gate and source lines 22 and 23 are formed over gate electrode 32 to form TFT 24.

In order for the teachings of SEO et al. to be relevant, the three layer structure of a common electrode 109 over the data electrode 108 over the gate bus line 101 would have to be implemented. Such teaching would increase the size (thickness) of the capacitor in TAGUSA et al. and would also require an additional step to form a common electrode such as electrode 109.

Column 7, lines 16-30 of TAGUSA et al. teach that the device of TAGUSA et al. simplifies the fabrication process such that the fabrication steps are not increased and the thickness of the device is not increased. As set forth above, the method of SEO et al. would require both an increase in process steps and an increased thickness. Since TAGUSA et al. teach away from these

features, one of ordinary skill in the art would not be motivated to combine SEO et al. with TAGUSA et al. to render obvious the claims of the present application.

Further, TAGUSA et al. teach microscopic hollows 28 that function as a collective lens which collect light incident from the underlying layers so that the light exits as columnated beams. As seen in Figure 2A of SEO et al., data electrode 108 and the common electrode 109 extend through the pixel region (defined between gate bus lines 101, 101' and data bus lines 102, 102'). Accordingly, not only would data electrode 108 and common electrode 109 add additional thickness to TAGUSA et al., which TAGUSA et al. teach the opposite, but these lines would also interfere with the operation of the microscopic hollows 28 of TAGUSA et al.

MPEP §2143.01 states that if a proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

The addition of data electrodes 108 and common electrodes 109 in the pixel region would affect the operation of the microscopic hollows of TAGUSA et al. and thus the proposed

combination of references is not sufficient to render the claims *prima facie* obvious.

An object of the present invention is to prevent "reverse tilt". Reverse tilt occurs when there is a lateral leak of electric field caused by the potential difference between gate lines and pixel electrodes. Neither TAGUSA et al. nor SEO et al. use a control electrode to prevent reverse tilt.

In fact, these references are concerned with light leakage and use two apparently disparate methods to prevent light leakage. Column 16, lines 1-16 and column 28, lines 21-48 of TAGUSA et al. teach that the overlap of the pixel electrode with the data lines in conjunction with the microscopic hollows blocks light leakage and improves the brightness and/or the viewing angle and thus the aperture ratio is improved. TAGUSA et al. teach that such method eliminates the necessity of forming a black mask on a counter substrate.

SEO et al. teach forming a black mask (black matrix 128) on the second substrate 111. Since TAGUSA et al. teach away from using a black matrix, one of ordinary skill in the art would not combine TAGUSA et al. with the teachings of SEO et al. which rely on the black matrix.

An object of SEO et al. is to use a three layer capacitor structure to increase the aperture ratio. This object of SEO et al. is achieved by having a black matrix preventing

light leakage over the gate bus line and the data bus line. As seen in Figures 3B-3D of SEO et al., the combination of the common electrode 119 and the data electrode 108 and the gate bus line 101 are rearranged to create different capacitive configurations. However, in each case the black matrix 128 overlies the capacitive structure to prevent leakage.

It is therefore not apparent why one of ordinary skill in the art would add the additional electrode structure of SEO et al. to TAGUSA et al. since this electrode structure does not prevent leakage; it is the black matrix that prevents leakage. Since TAGUSA et al. teach away from using a black matrix, it is also not apparent why one of ordinary skill in the art would be motivated to combine SEO et al. with TAGUSA et al.

In any event, it is not apparent that the proposed combination of references would prevent the lateral leak of the electrical field caused by the potential difference between gate lines and pixel electrodes such that one of ordinary skill in the art attempting to prevent this occurrence would look to these references for this teaching.

Accordingly, claims 1-4, 10-16, 18, 19, 21 and 22 are believed patentable over the proposed combination of references.

Claims 5-9, 17 and 20 are rejected as unpatentable over TAGUSA et al. in view of SEO et al. and applicants'

disclosed prior art and further in view of YAO et al. 5,682,211. This rejection is respectfully traversed.

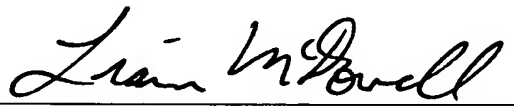
YAO et al. is only cited for the teaching of a control electrode having the same potential voltage as a source electrode. YAO et al. do not teach or suggest what is recited in claims 1 and 16. As set forth above, the combination of TAGUSA et al., SEO et al. and applicants' disclosed prior art do not teach or suggest what is recited in claims 1 and 16. Since claims 5-9, 17 and 20 depend from one of claims 1 and 16 and further define the invention, the proposed combination of references would not render obvious claims 5-9, 17 and 20.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R.§1.17.

Respectfully submitted,

YOUNG & THOMPSON



Liam McDowell, Reg. No. 44,231
745 South 23rd Street
Arlington, VA 22202
Telephone (703) 521-2297
Telefax (703) 685-0573
(703) 979-4709

LM/lrs